**Module Behavior Simulation**

(1) Control logic for Comp FSM (conv2x1 3/5x1 and FC)

Promote: Merge control logic for psum update into comp FSM

(2) Control logic for DDR <-> SRAM, SRAM->REG

(3) Control logic for Ping-Pong weight load

(4) Promote: Buffer non-linear activation function parameter in REG

**SoC Architecture**

(1) Mesh (2) Cascade

 

**Bug**

(1) When process odd sequences, the tail of the input is not gated.