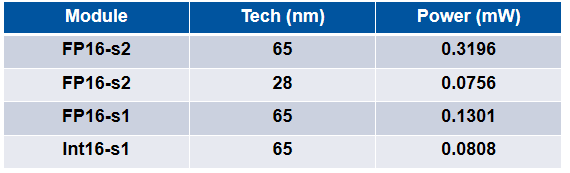
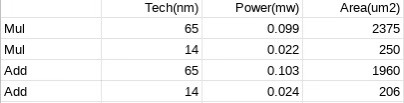
**Accomplishment**

1. Synthesize FP16 multiplier and adder with 65nm, 28nm and 14nm (400MHz, 100MHz).





Result: Booth-coding-type addition (distributing addition into four cycles) causes high latency and low energy efficiency.

2. Finish DLA computing-part RTL.

PE array + Reconfigurable post process engine

3. Simulate computing-part RTL with pseudo data.

**Plan**

DLA control-part RTL

**TODO**

1. C-version DLA model for test case generation and compromise among data format, intermediate results register length and accuracy.

2. SOC bridge.